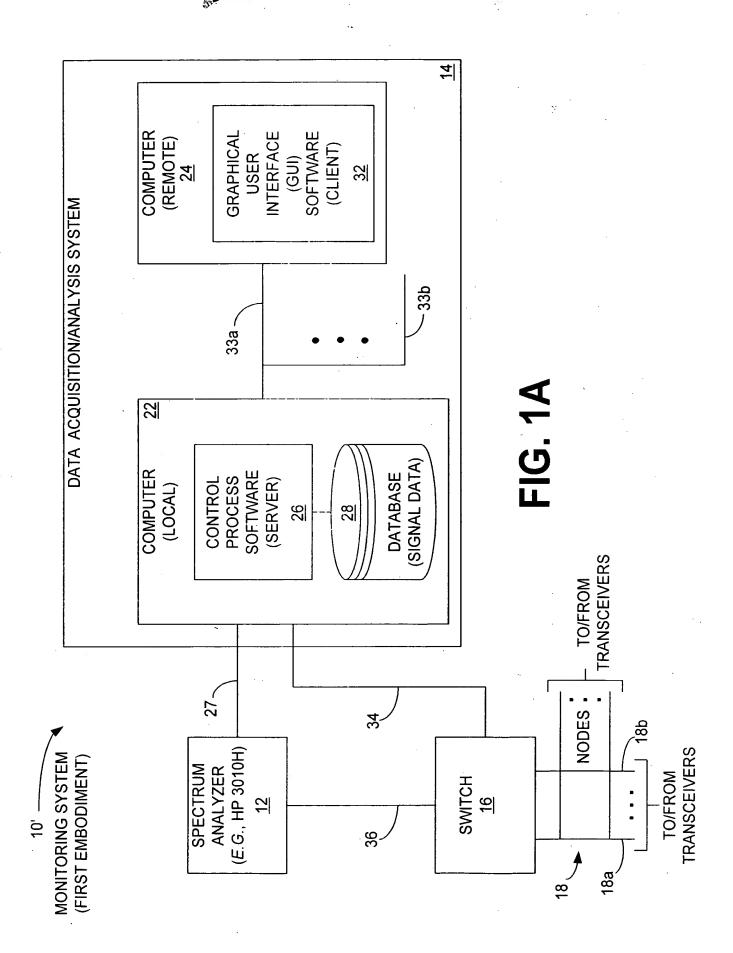
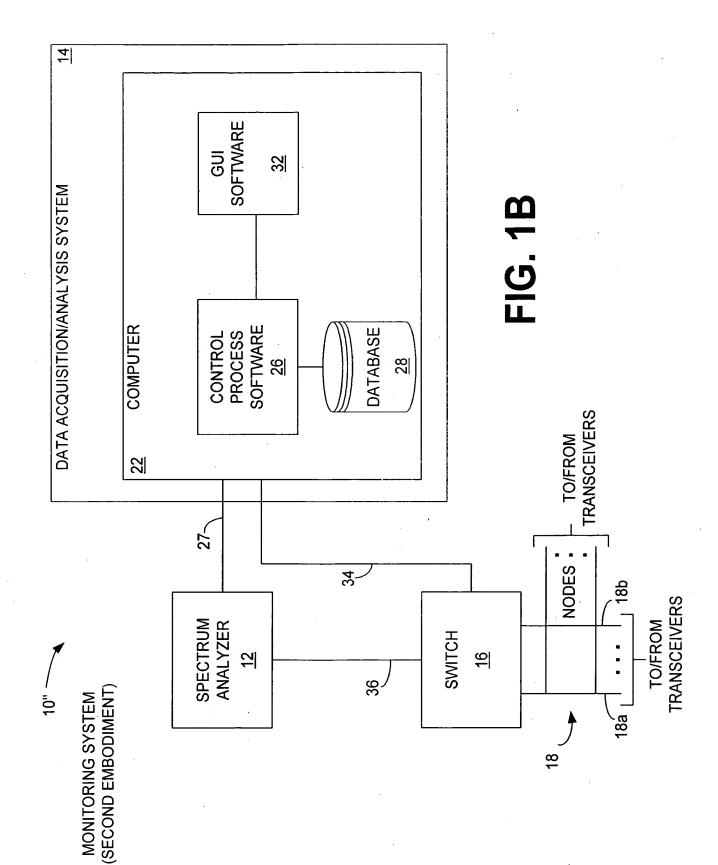
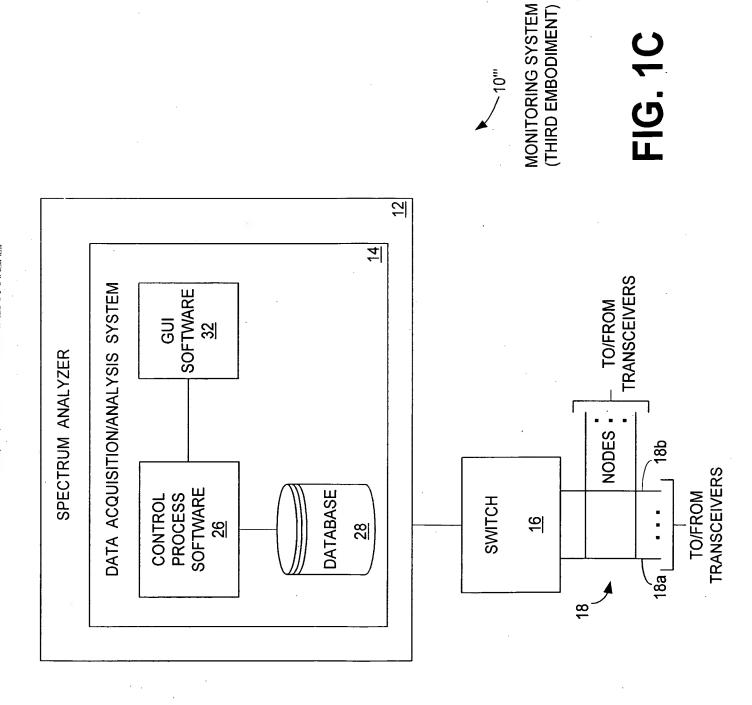
E -11







CHANNEL D 52 CHANNEL TEST PLAN Y CHANNEL C **DEVICE 2** CHANNEL B CHANNEL A CHANNEL TEST PLAN X **FIG. 2** TEST PLAN(S) **DEVICE 1** DATA STRUCTURE OF DATABASE 62-58, 64" **CHANNEL PLAN A** WHOLE NODE TEST PLAN A 64. 56-64-CHANNEL B TEST RESULTS CHANNEL C TEST RESULTS CHANNEL D TEST RESULTS **TEST RESULTS TEST RESULTS** WHOLE NODE NODE CHANNEL A 89 **TEST RESULTS** 54 68,

CHANNEL PLAN

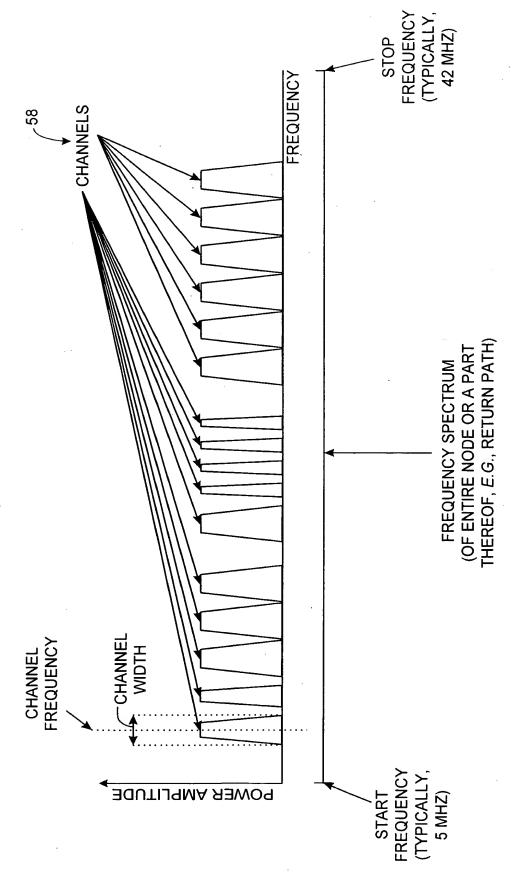
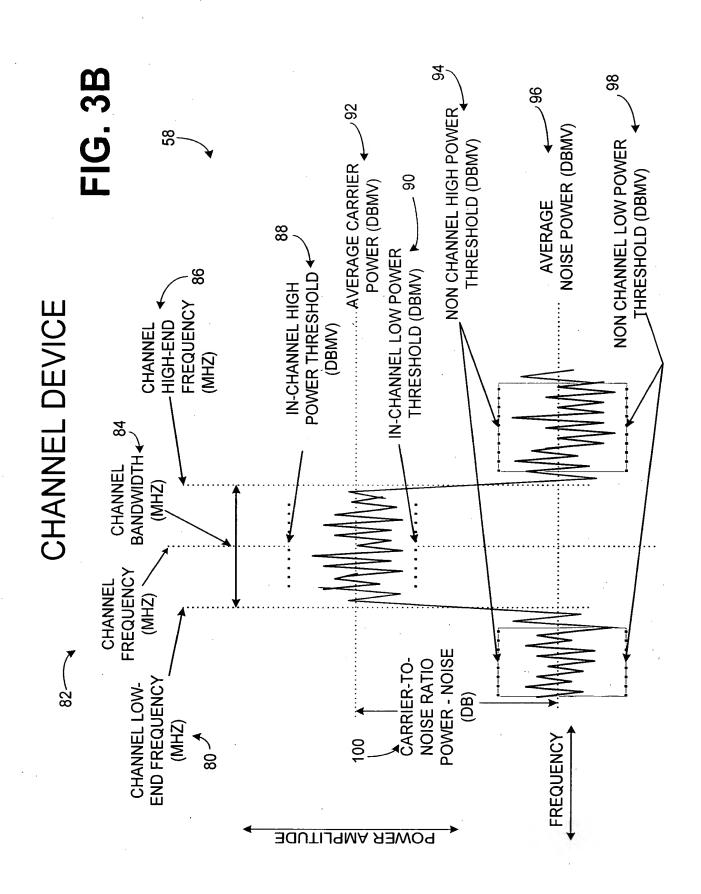


FIG. 3A



TEST PLAN

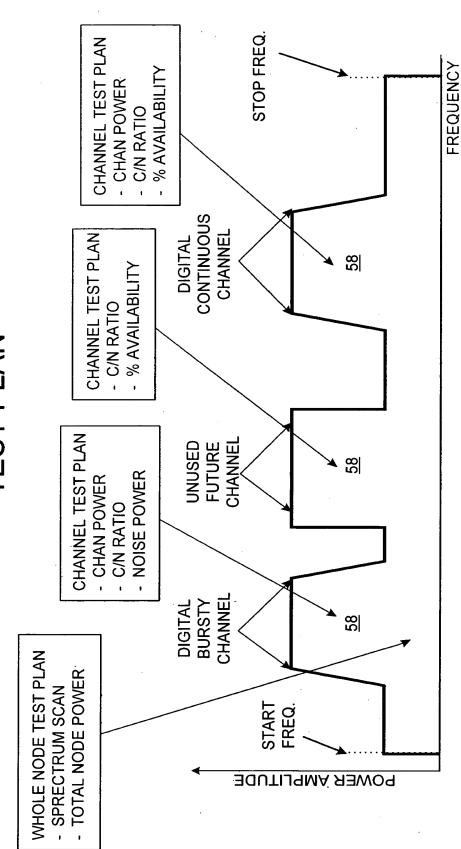


FIG. 3C

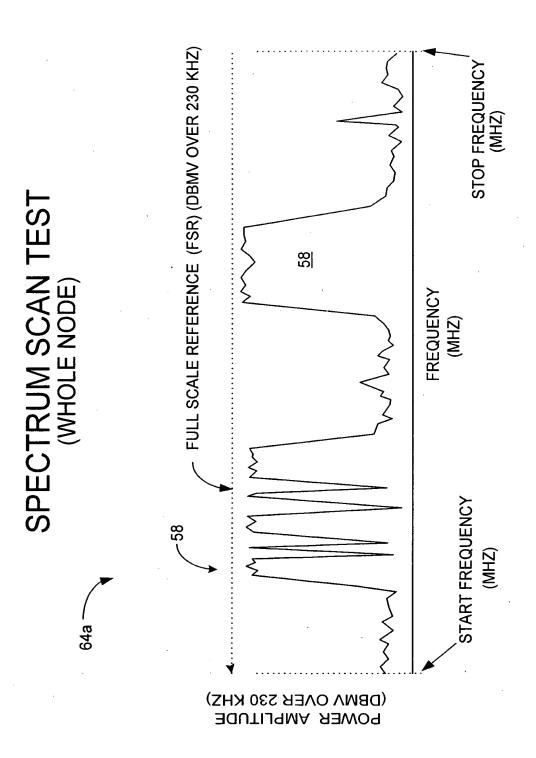


FIG. 3D

SPECTRUM SCAN TEST (ALARM LIMITS)

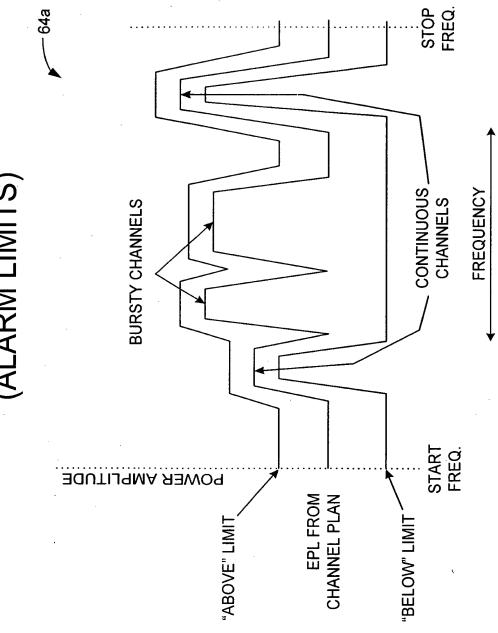


FIG. 3E

TOTAL NODE POWER TEST (WHOLE NODE)

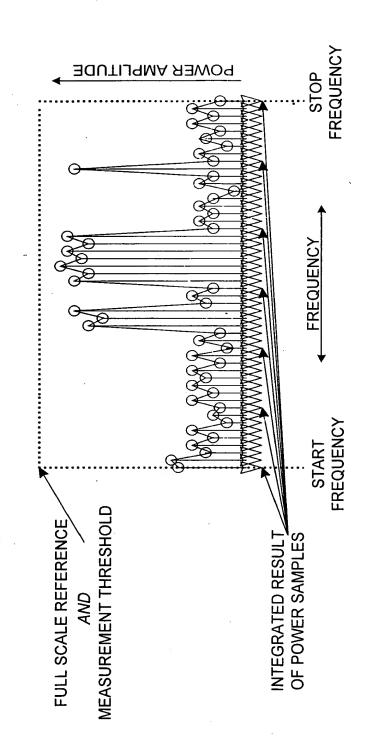


FIG. 3F

AVERAGE NOISE POWER TEST (CHANNEL)

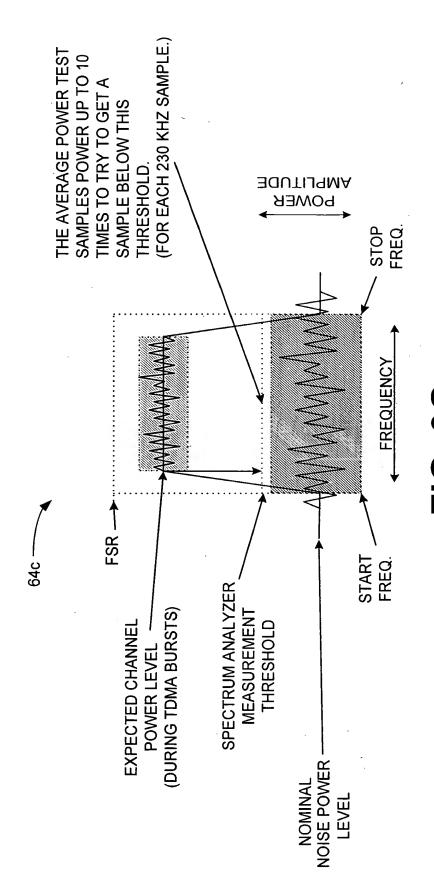


FIG. 3G

AVERAGE NOISE POWER TEST (ALARM LIMITS)

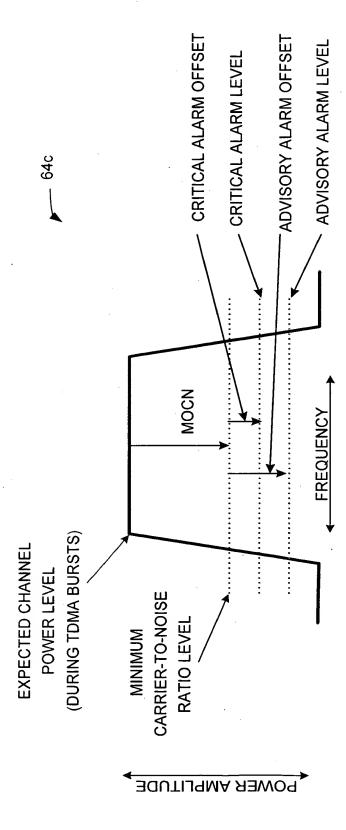


FIG. 3H

CHANNEL POWER TEST (CHANNEL)

64d —

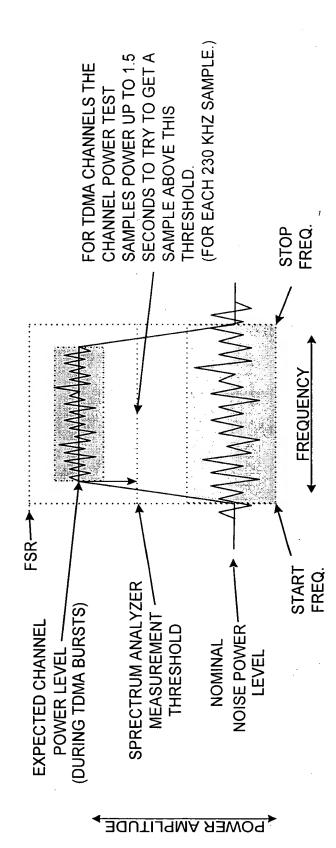


FIG. 3

CHANNEL POWER TEST (ALARM LIMITS)

64q

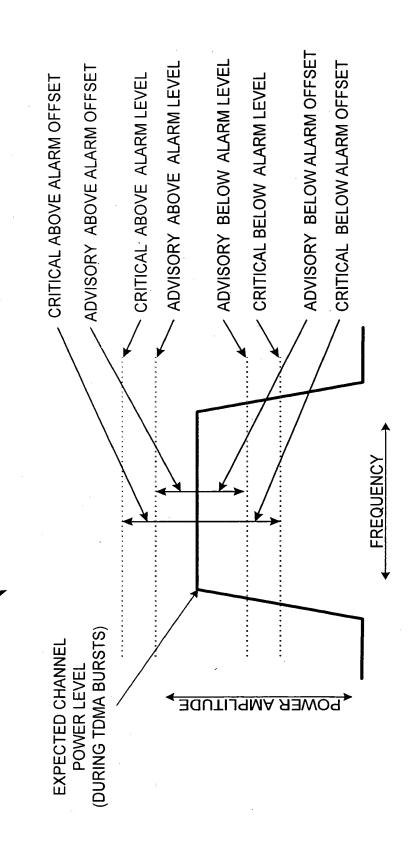


FIG. 3J

CHANNEL POWER TEST 1.5 SEC DWELL (TDMA BURSTS) M M MARAN 0.2 S DWELL MEASUREMENT THRESHOLD

POWER AMPLITUDE

FIG. 3K

C/N TEST (CHANNEL)

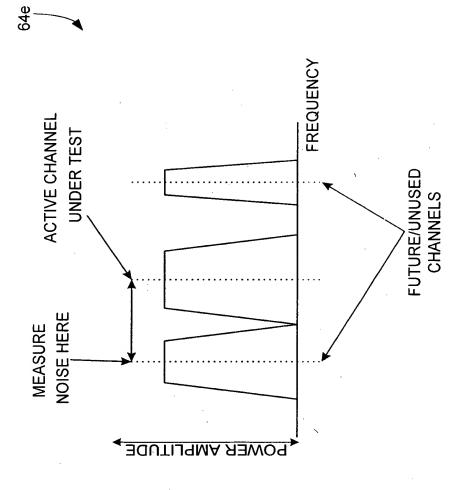


FIG. 3L

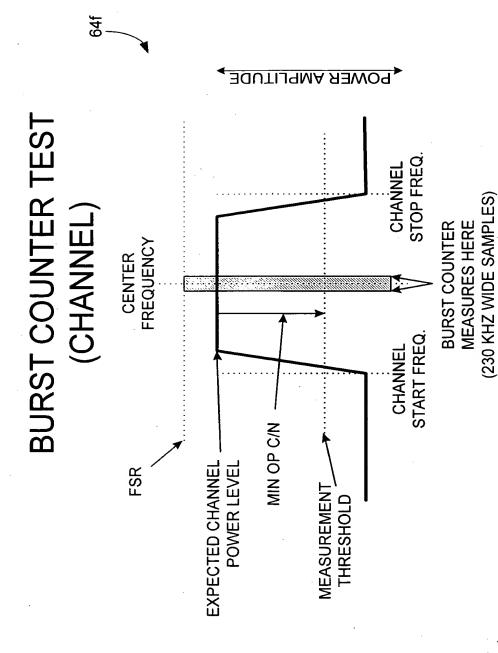


FIG. 3M

FREQUENCY

PERCENT AVAILABILITY TEST (CHANNEL)

- **64**g

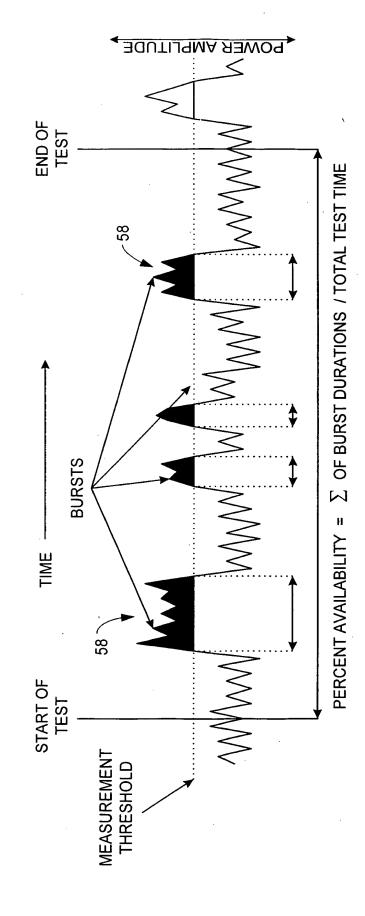


FIG. 3N

PERCENT AVAILABILITY TEST (ACTIVE CHANNELS)

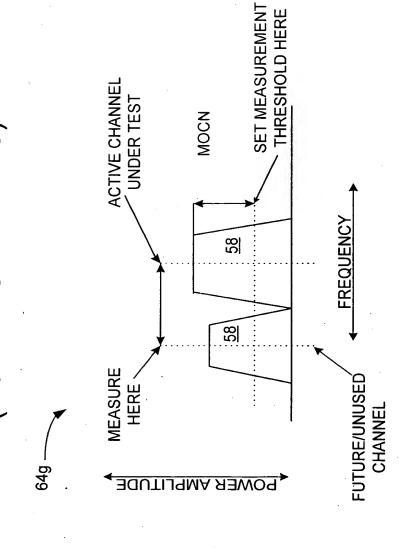


FIG. 30

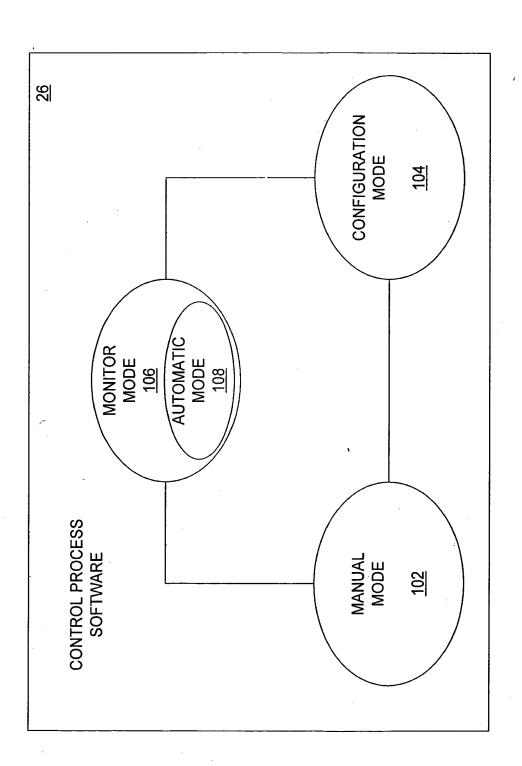


FIG. 4

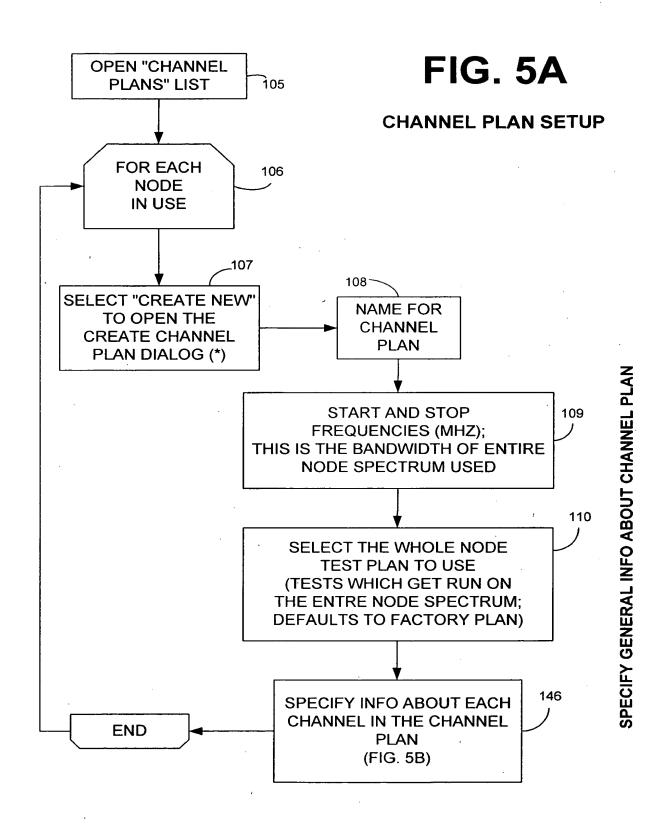
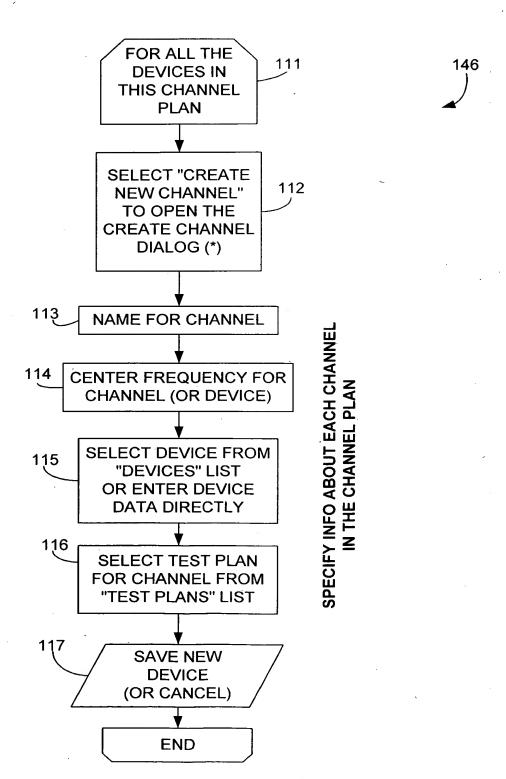
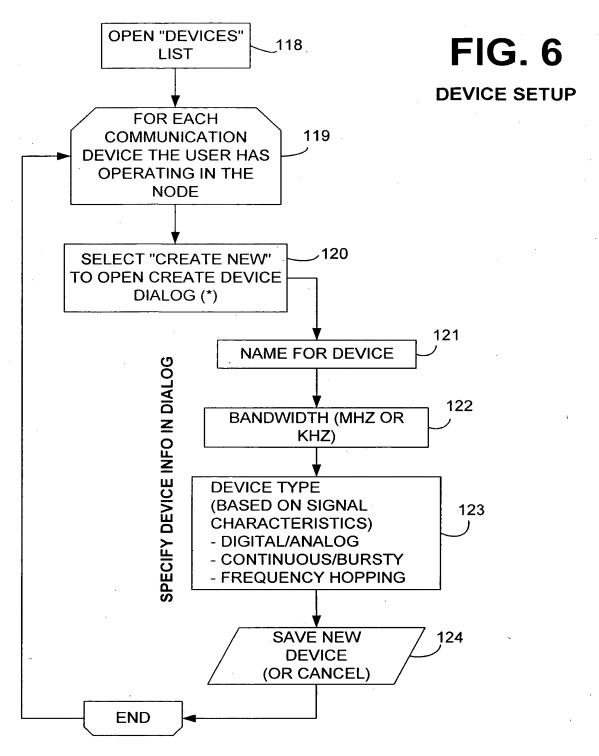


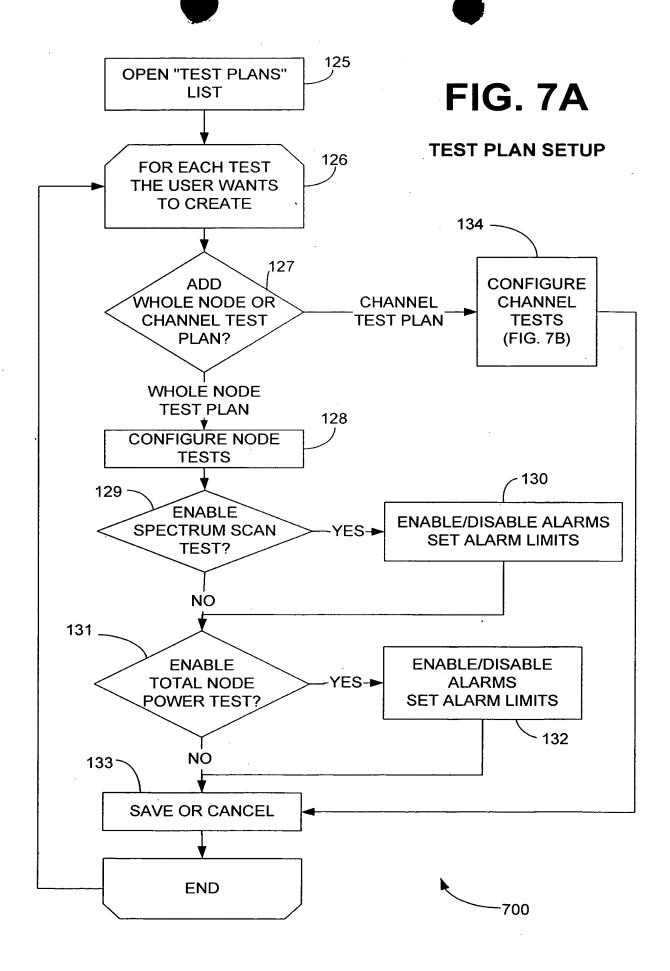
FIG. 5B

CHANNEL PLAN SETUP (CONTINUED)





* NOTE: DEVICE LIST DIALOG ALSO ALLOWS USER TO EDIT OR DELETE DEVICES.



TEST PLAN SETUP (CONTINUED)

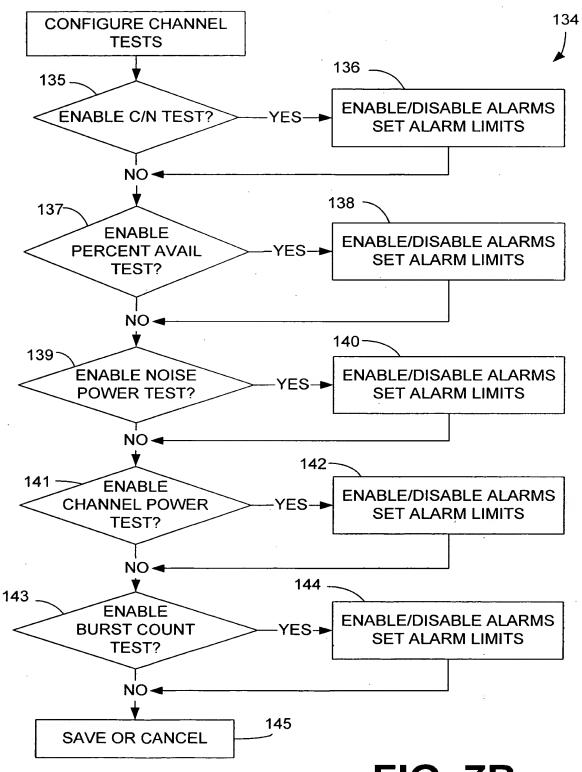
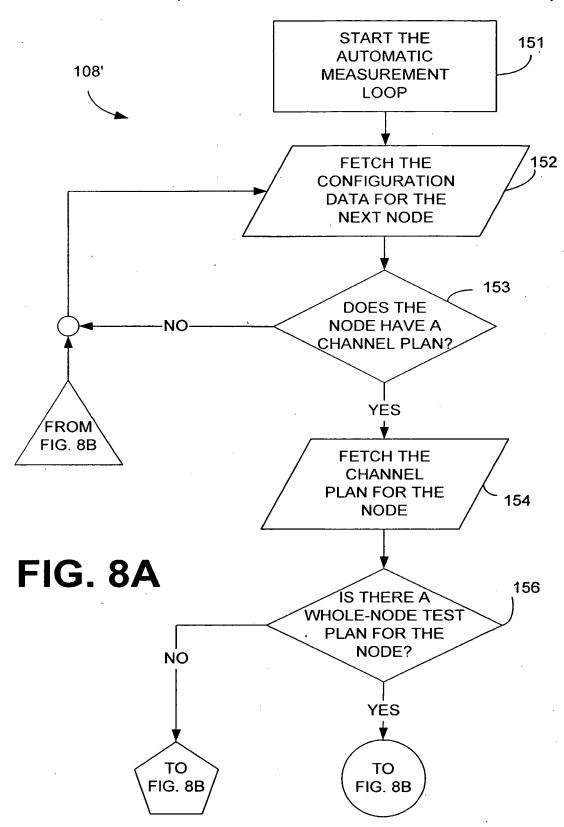
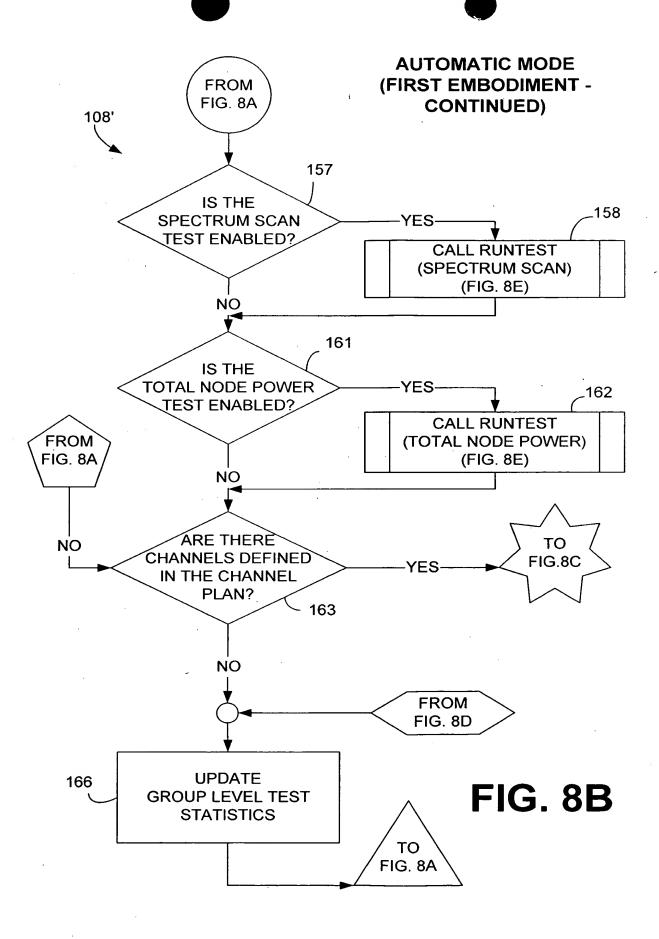
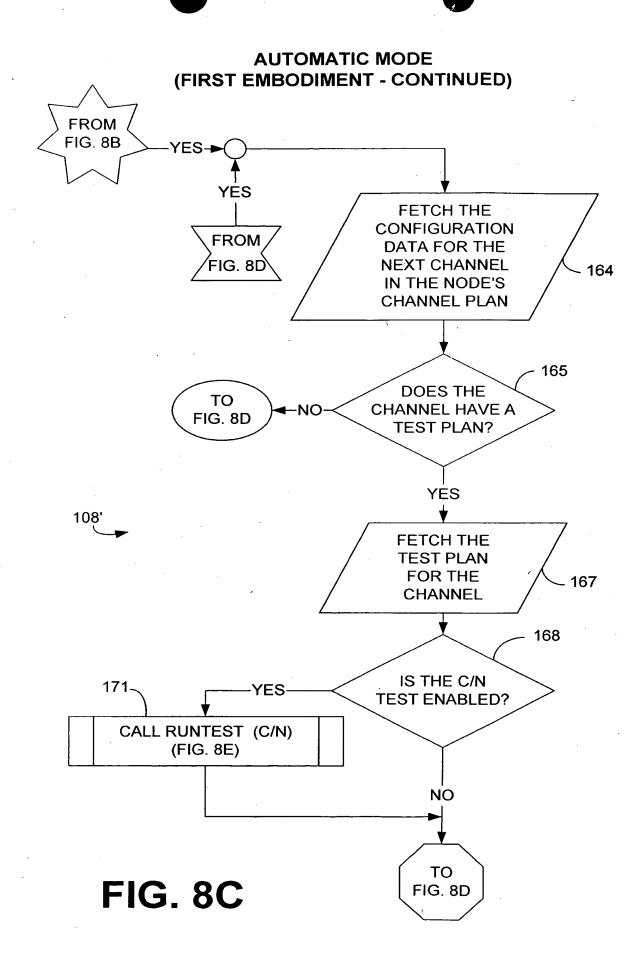


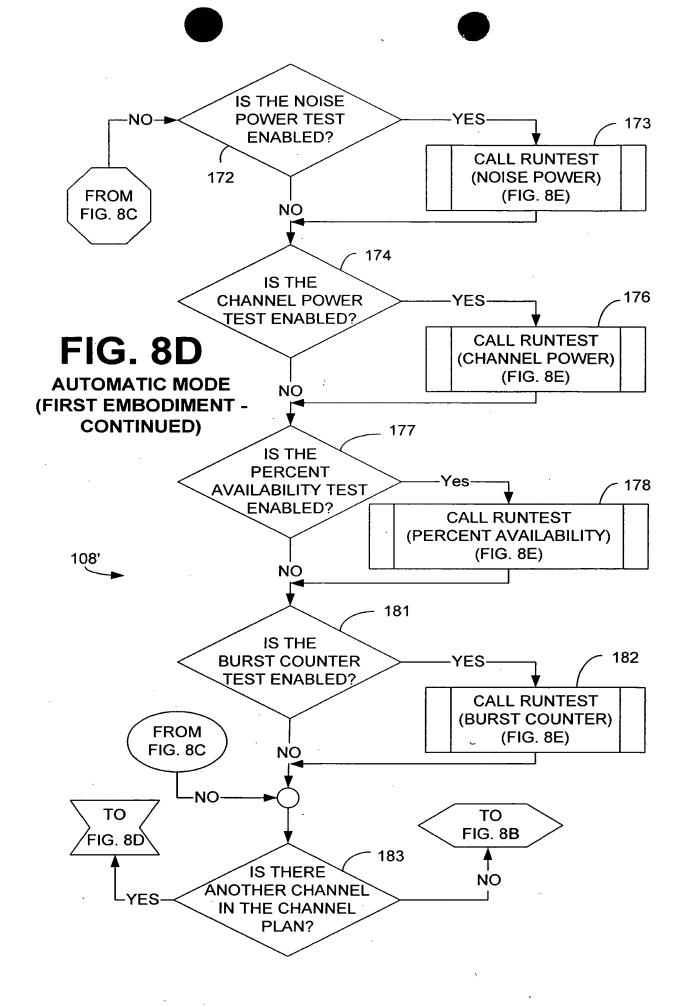
FIG. 7B

AUTOMATIC MODE (FIRST EMBODIMENT; EMPLOYS ROUND ROBIN ALGORITHM)

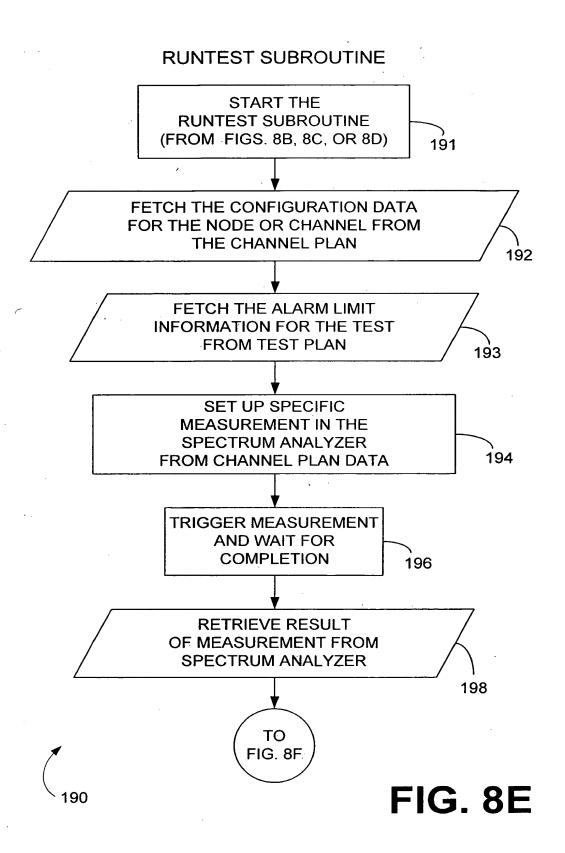




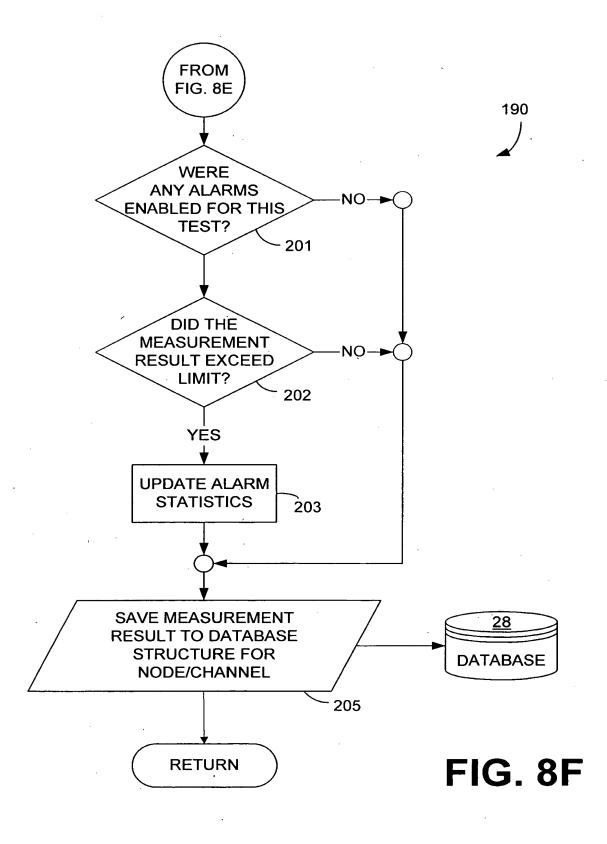




AUTOMATIC MODE (FIRST EMBODIMENT - CONTINUED)



AUTOMATIC MODE (FIRST EMBODIMENT - CONTINUED)



AUTOMATIC MODE (SECOND EMBODIMENT; EMPLOYS SMART SCANNING ALGORITHM)

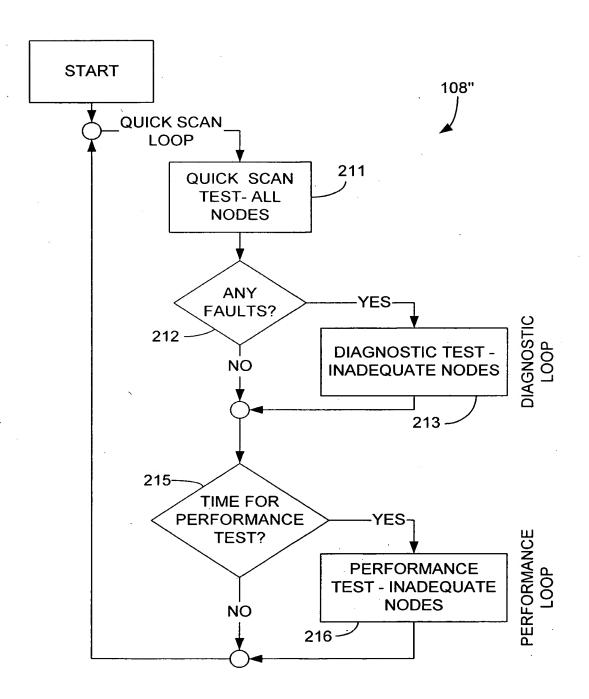
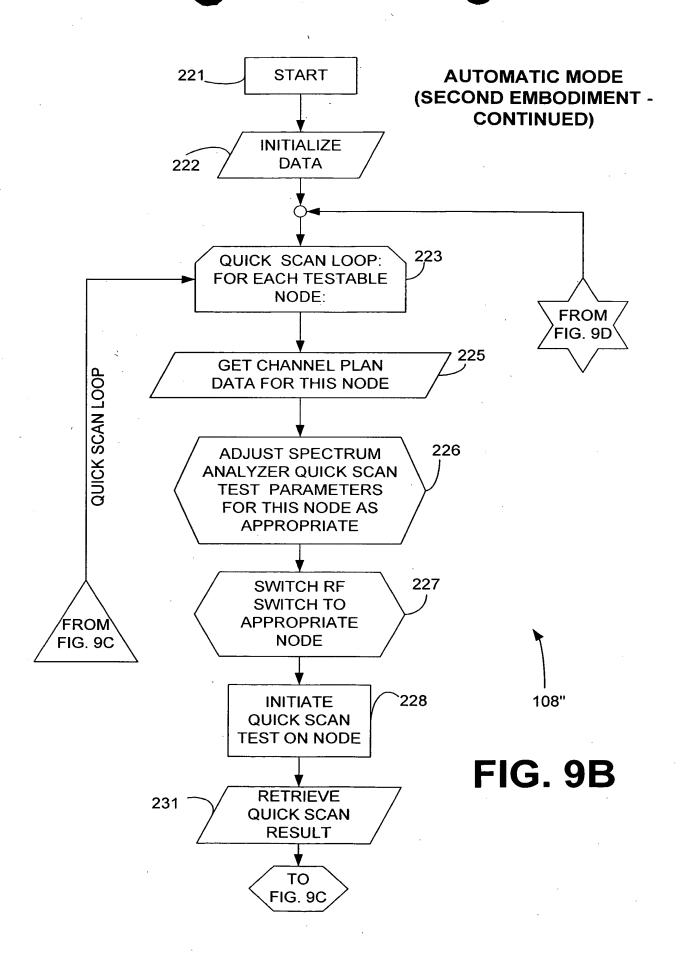
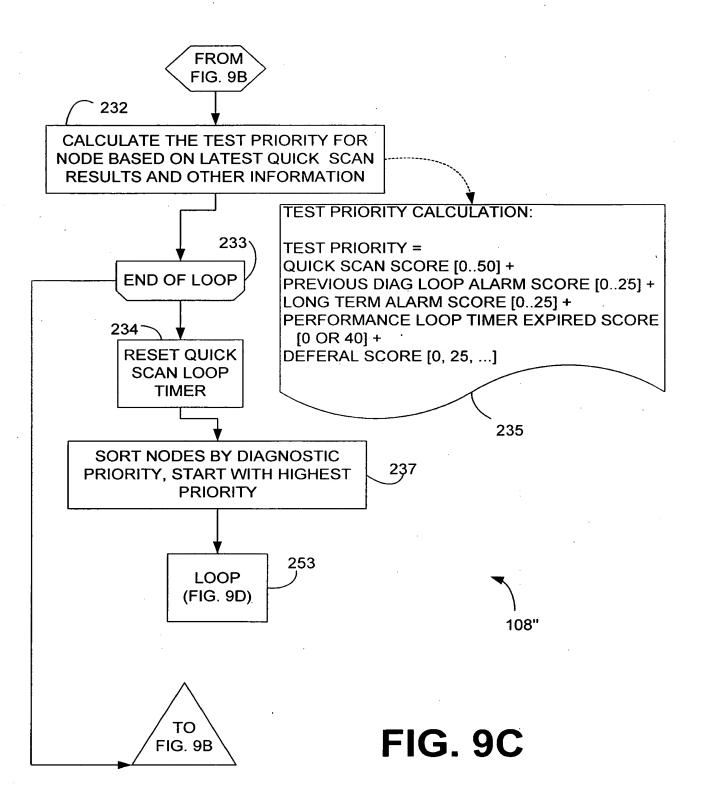


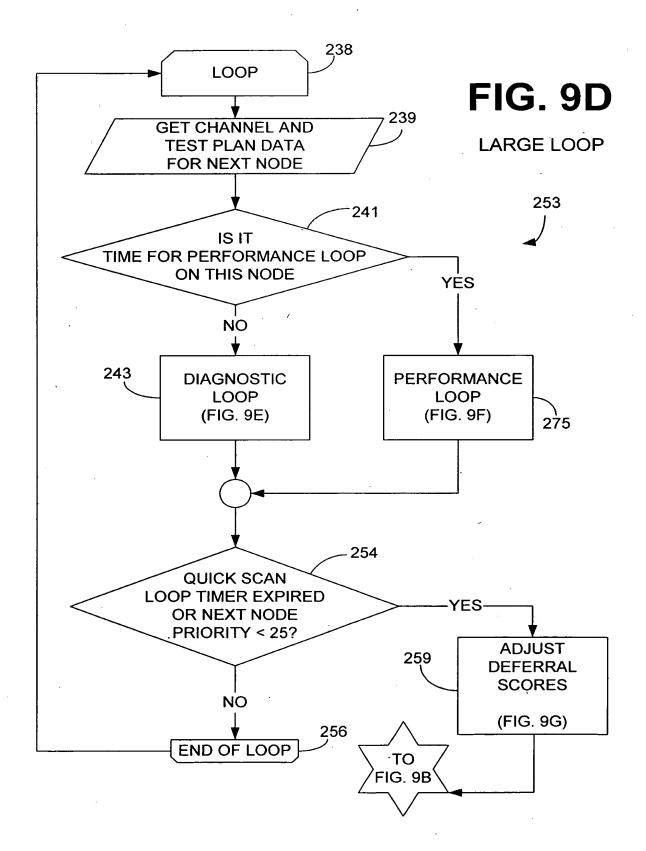
FIG. 9A



AUTOMATIC MODE (SECOND EMBODIMENT - CONTINUED)



AUTOMATIC MODE (SECOND EMBODIMENT - CONTINUED)



AUTOMATIC MODE (SECOND EMBODIMENT - CONTINUED)

DIAGNOSTIC LOOP

243 -

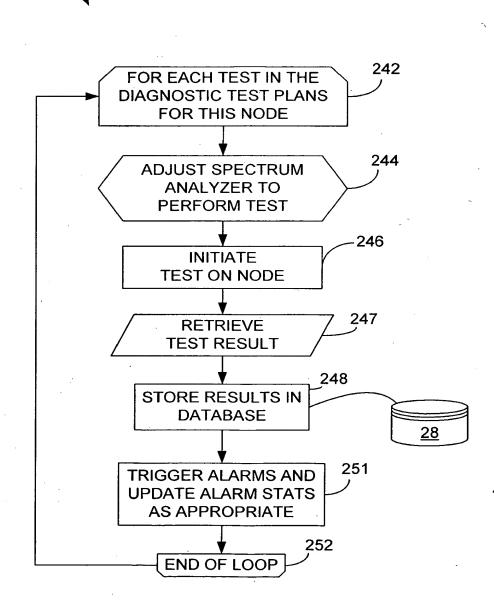
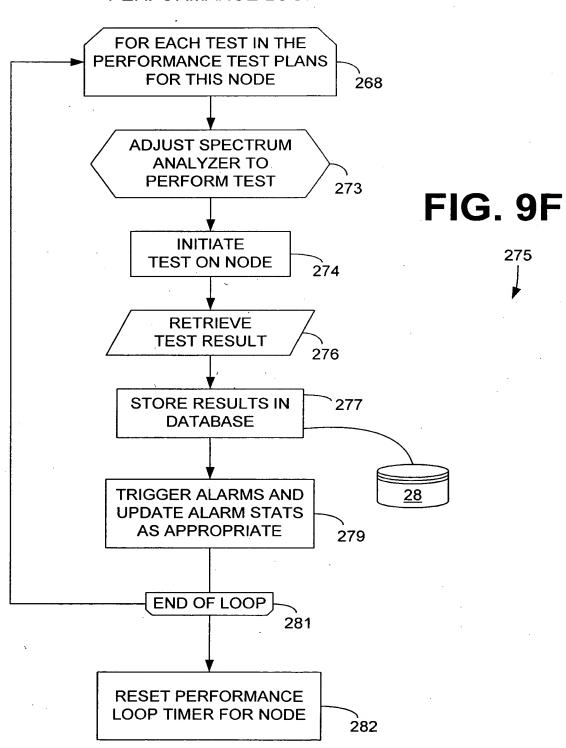


FIG. 9E

AUTOMATIC MODE (SECOND EMBODIMENT - CONTINUED)

PERFORMANCE LOOP



AUTOMATIC MODE (SECOND EMBODIMENT - CONTINUED)

ADJUST DEFERAL SCORES LOOP

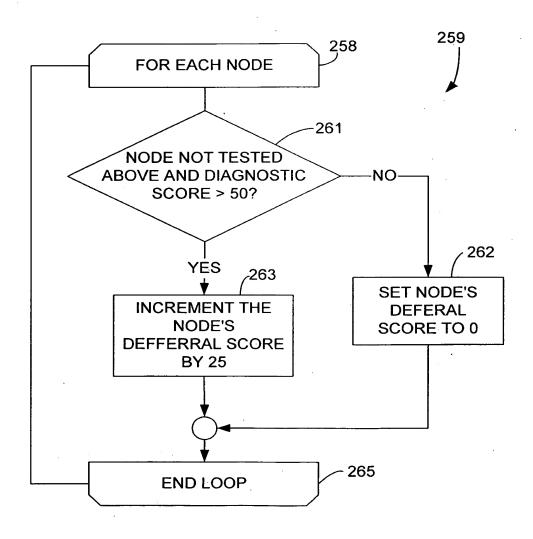
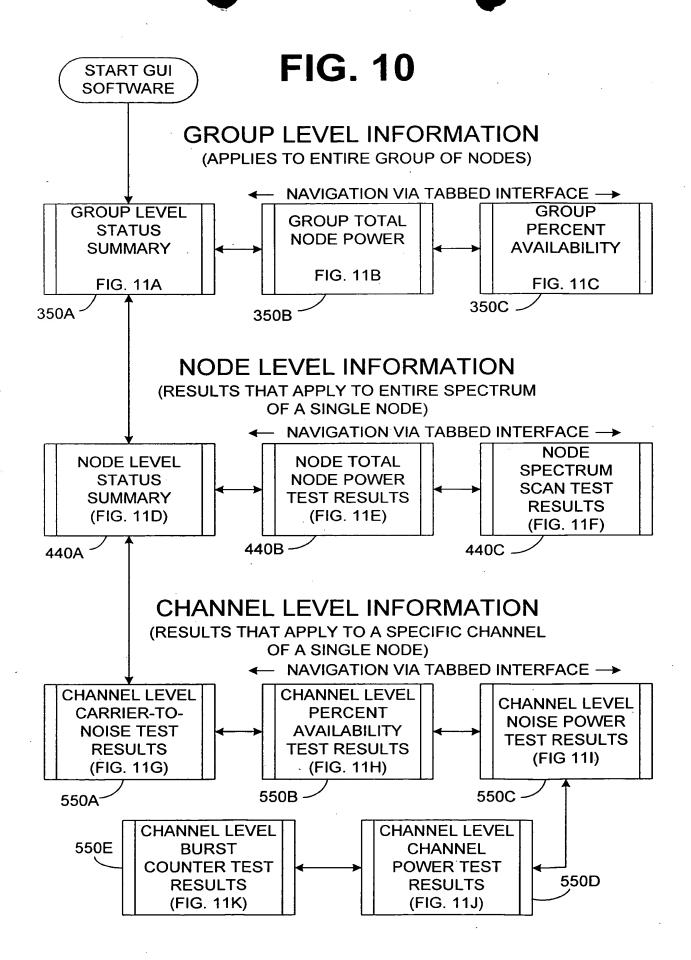
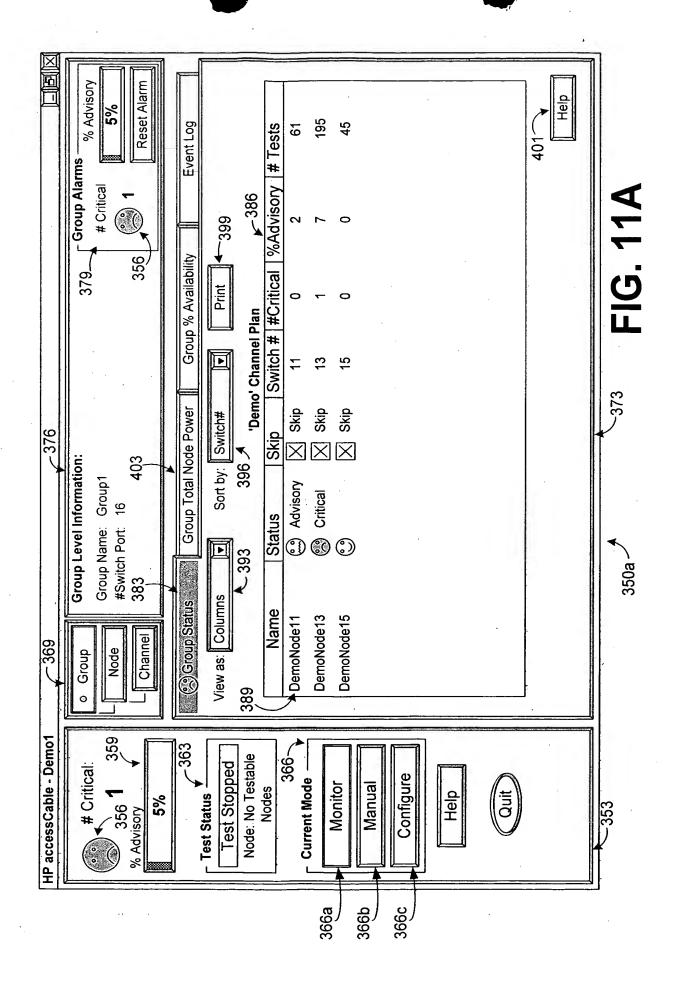
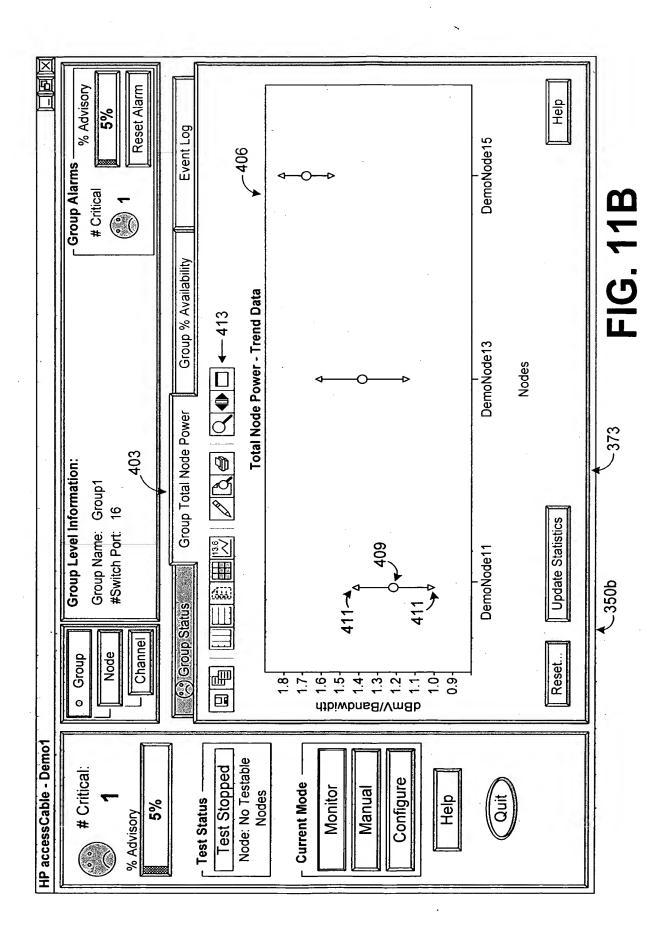
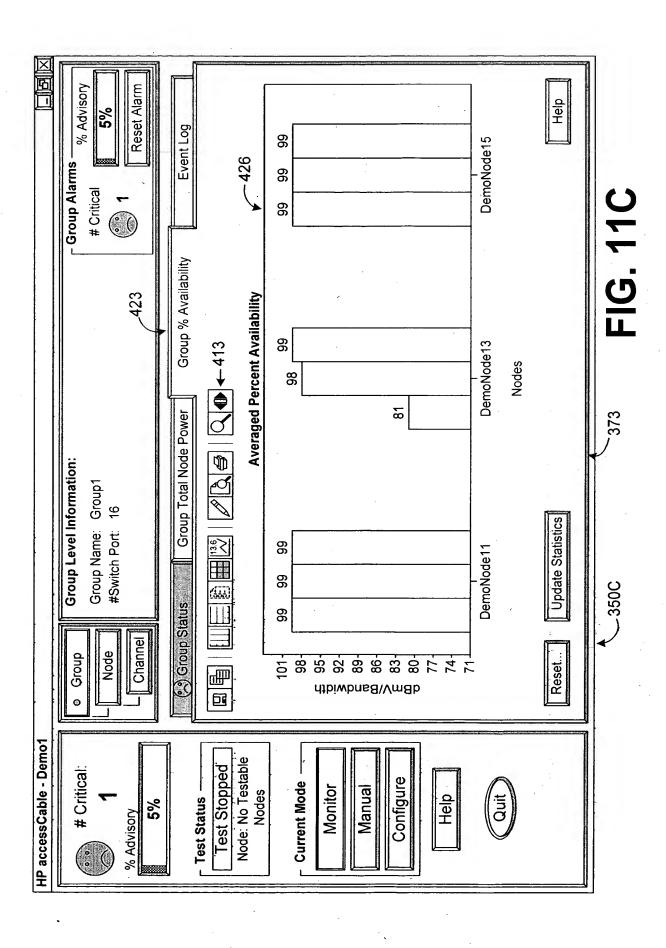


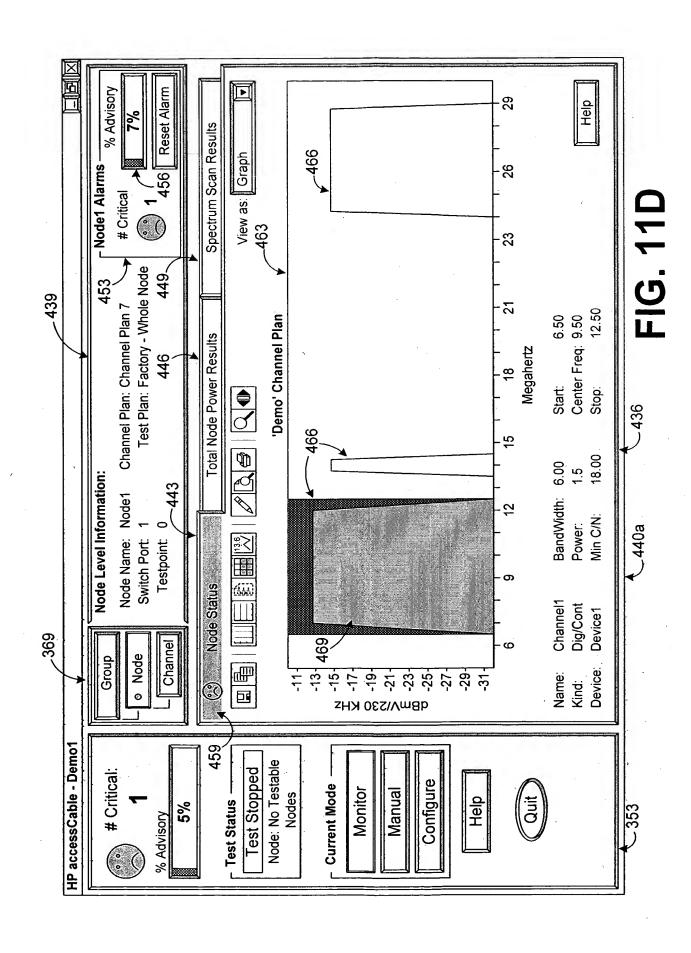
FIG. 9G

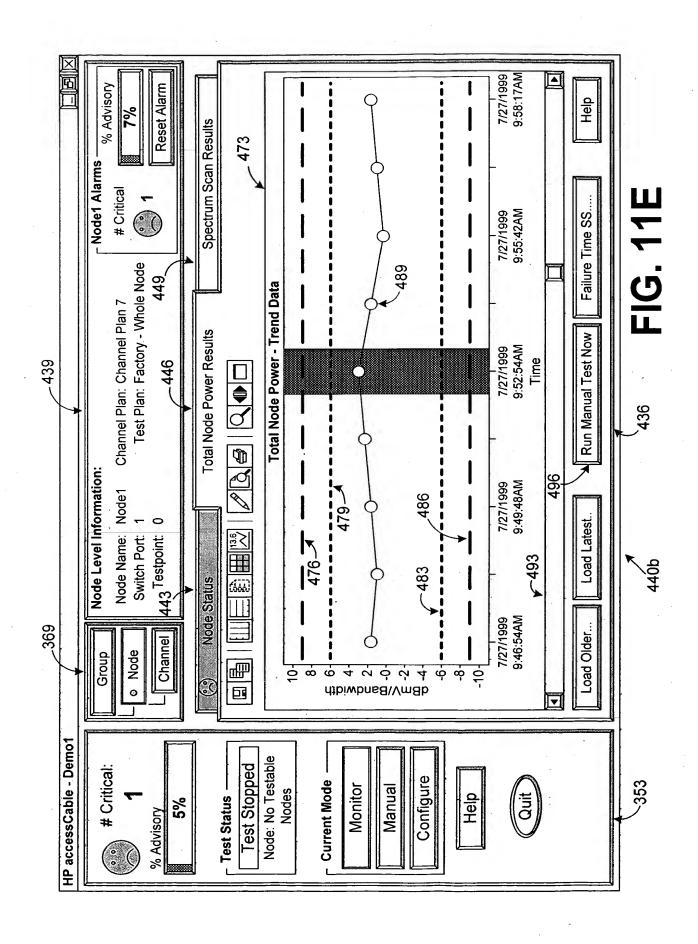


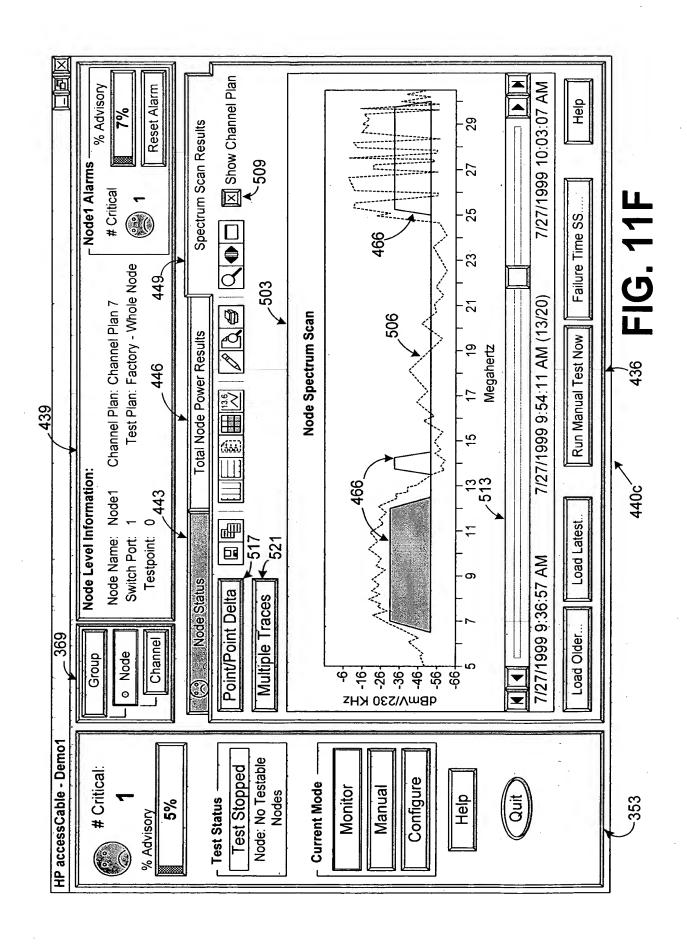


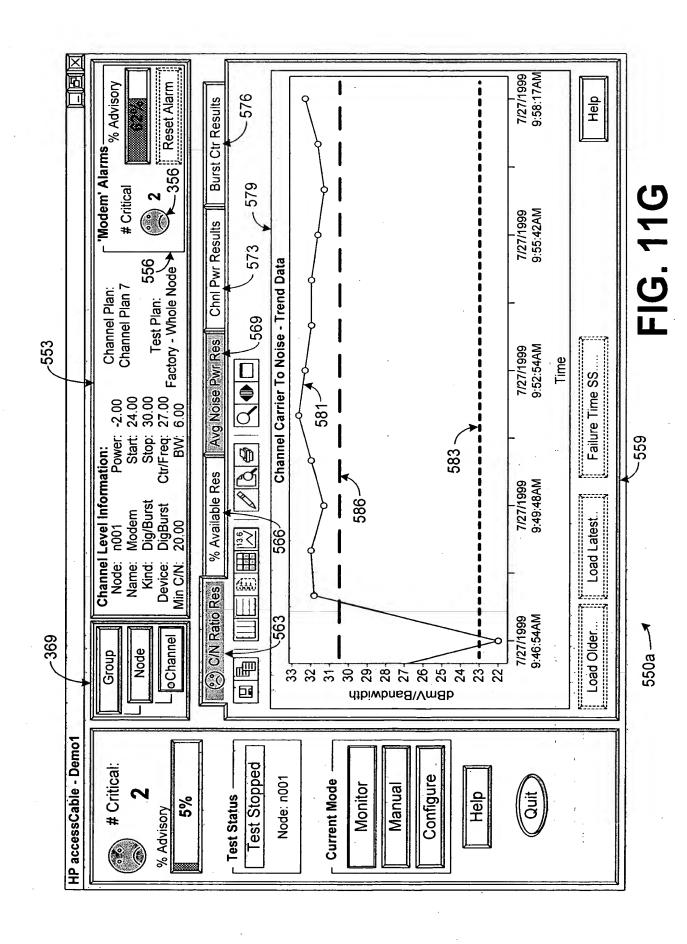


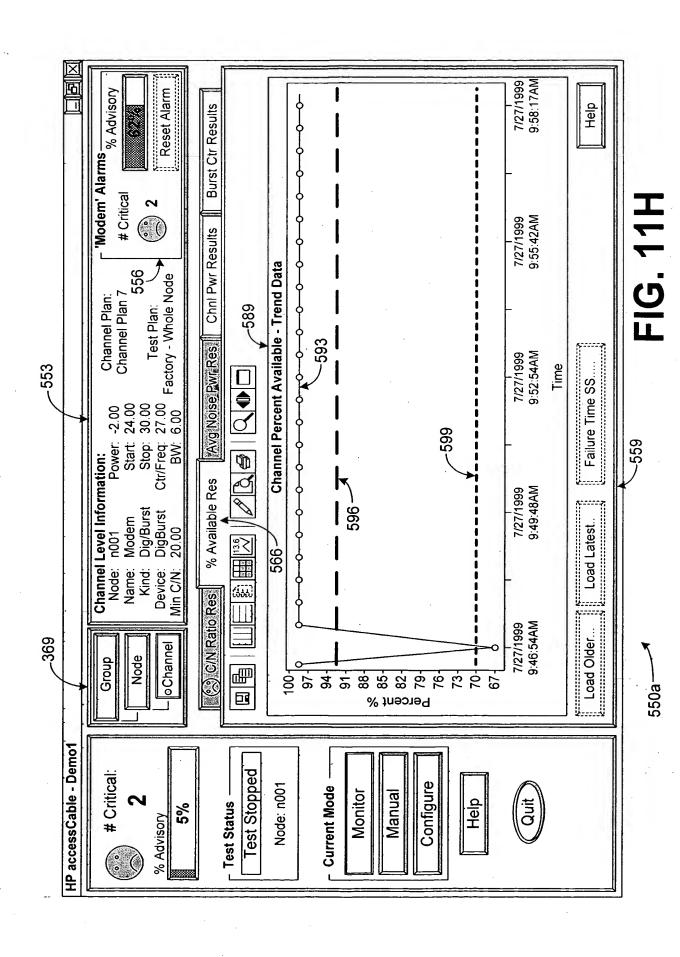












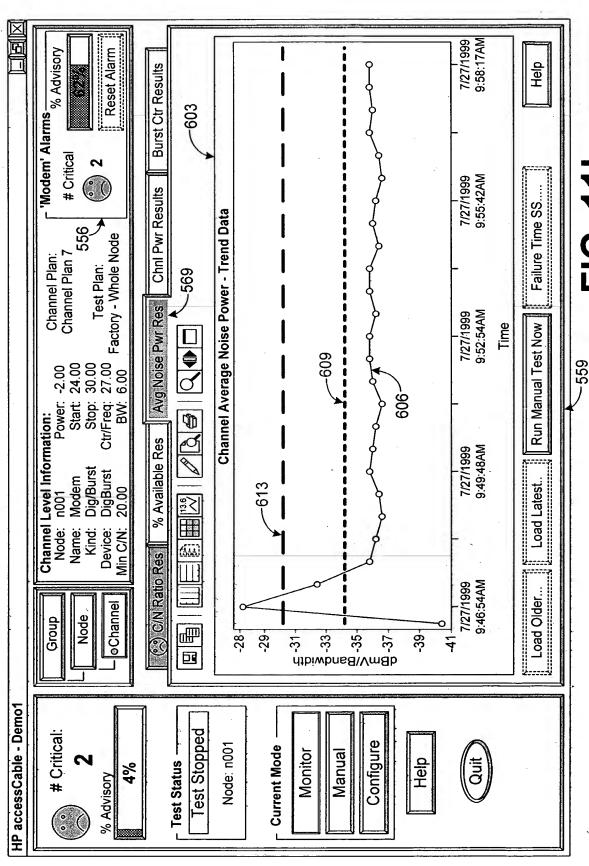
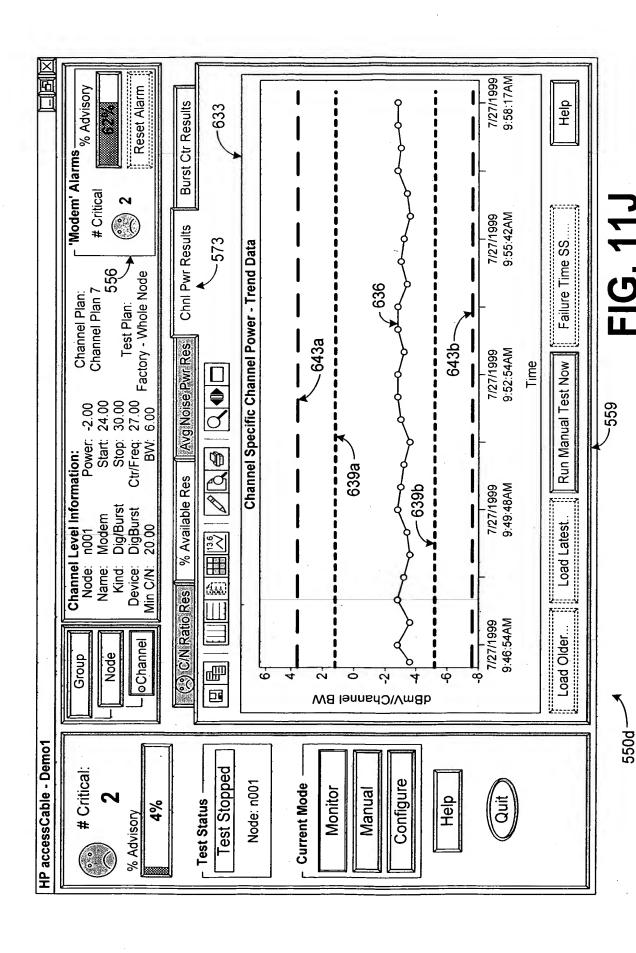


FIG. 111

550c



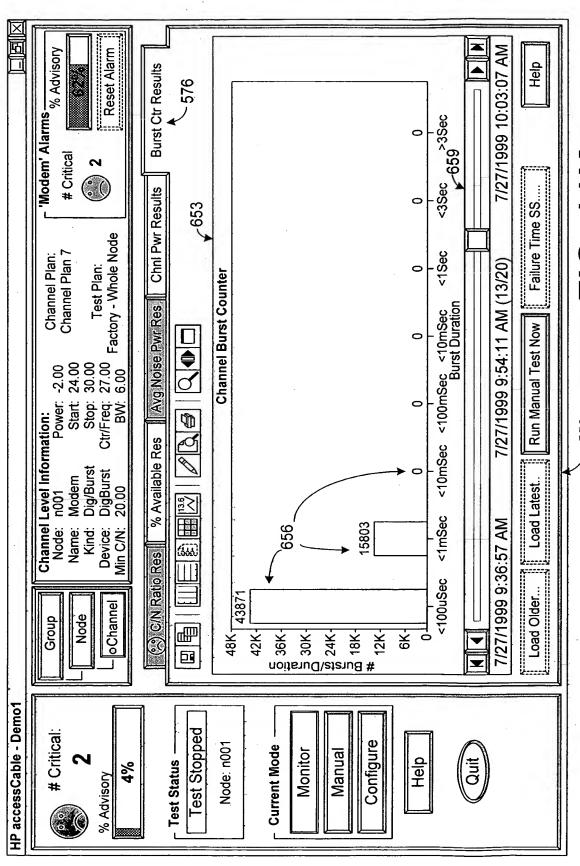


FIG. 11K

550e

TEST CONFIGURATION GUI NAVIGATION

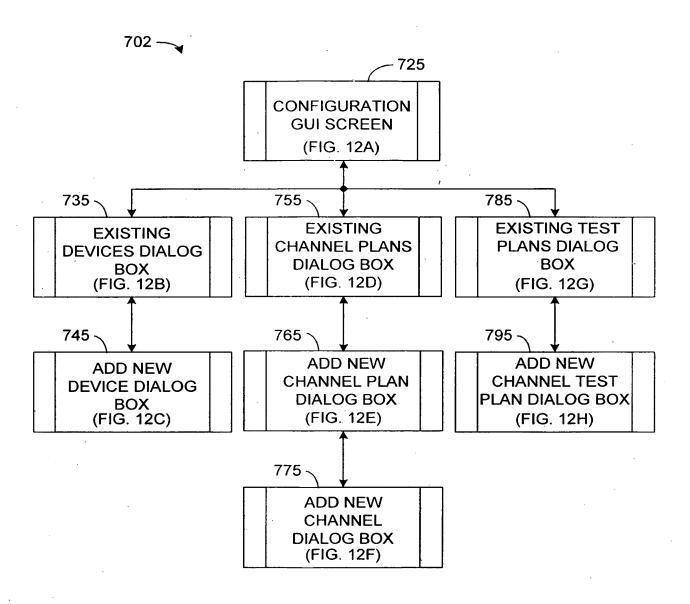


FIG. 12

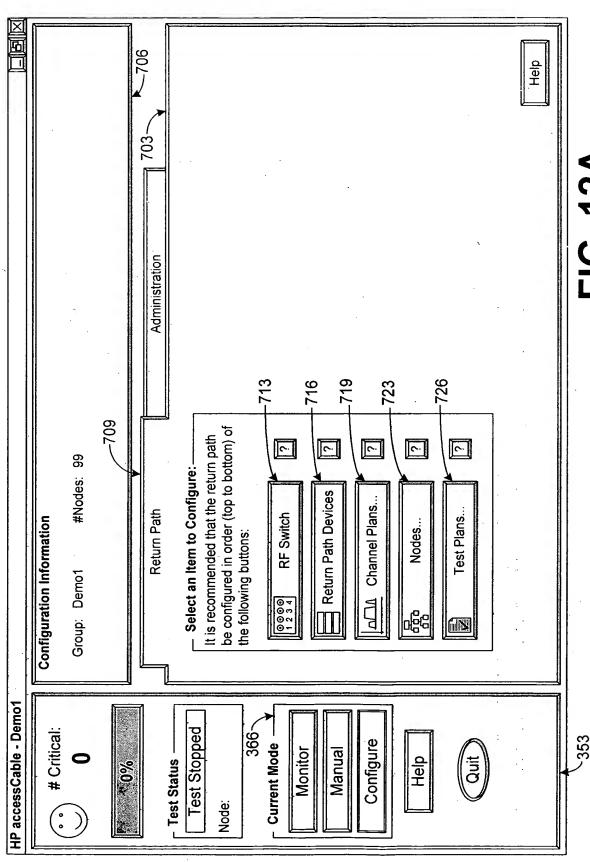


FIG. 12A

7007

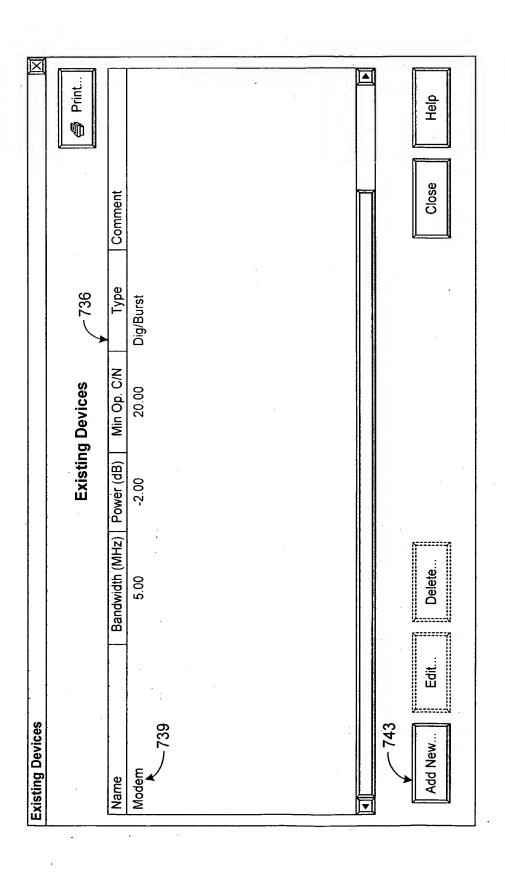


FIG. 12B

733 -

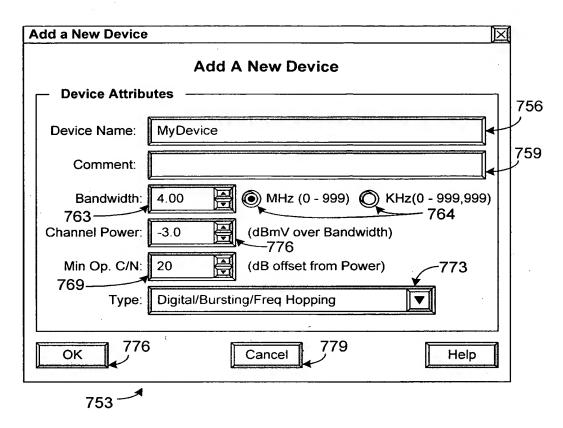


FIG. 12C

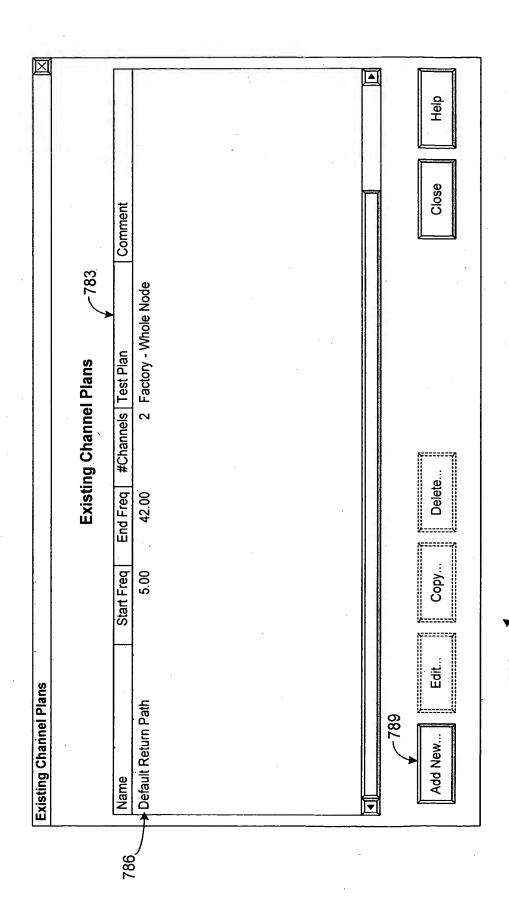


FIG. 12D

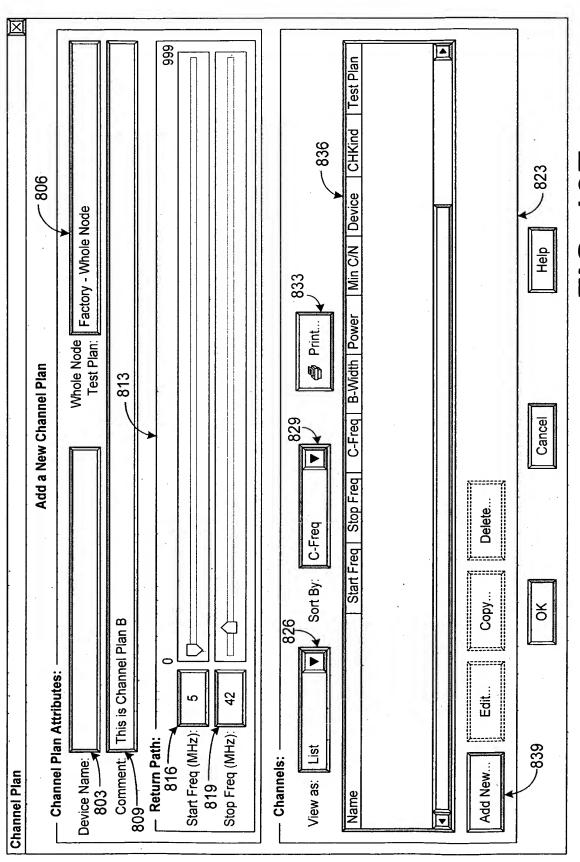


FIG. 12E

800

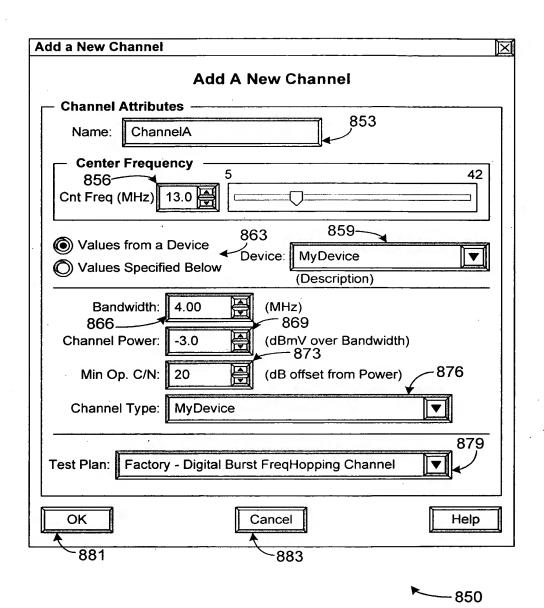


FIG. 12F

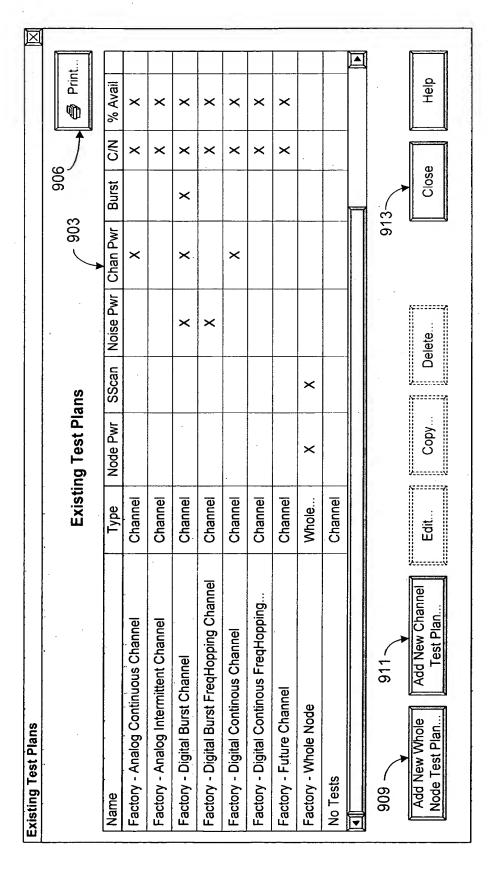


FIG. 12G

900

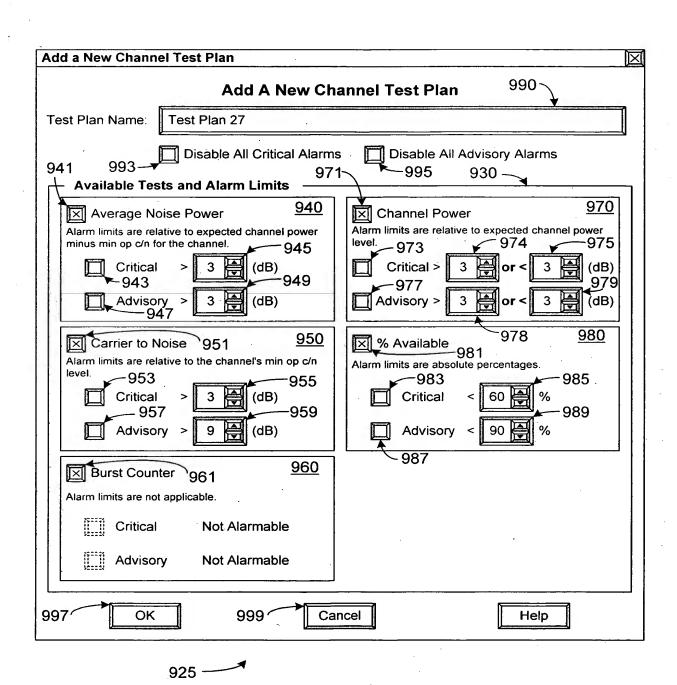


FIG. 12H